CLAIMS

What is claimed is:

1. An integrated circuit comprising:

one or more functional blocks to perform one or more functions; and

an on-chip frequency compensation circuit including

a selectively enabled reliability oscillator to generate a reference oscillating signal,

a clocked reliability oscillator to generate an AC degraded oscillating signal, and

a compare circuit coupled to the reliability oscillators, the compare circuit to compare the oscillating signals and to generate a frequency compensation signal in response to the comparison being greater than a predetermined threshold.

2. The integrated circuit of claim 1, wherein

the on-chip frequency compensation circuit further includes

a first counter coupled between the selectively enabled reliability oscillator and the compare circuit, the first counter to generate a reference count;

a second counter coupled between the clocked reliability oscillator and the compare circuit, the second counter to generate a dynamic count; and

the compare circuit to compare the reference count with the dynamic count.

3. The integrated circuit of claim 2, wherein

the on-chip frequency compensation circuit further includes

a first prescaler coupled between the selectively enabled reliability oscillator and the first counter, the first prescaler to divide by N the number of oscillations in an oscillating signal from the selectively enabled reliability oscillator; and

a second prescaler coupled between the dynamic reliability oscillator and the second counter, the second prescaler to divide by N the number of oscillations in an oscillating signal from the dynamic reliability oscillator.

4. The integrated circuit of claim 1, wherein

the on-chip frequency compensation circuit further includes

a static reliability oscillator to generate a DC bias degraded oscillating signal.

5. The integrated circuit of claim 4, wherein the on-chip frequency compensation circuit further includes

a first counter coupled between the selectively enabled reliability oscillator and the compare circuit, the first counter to generate a reference count;

a second counter coupled between the clocked reliability oscillator and the compare circuit, the second counter to generate a dynamic count;

a third counter coupled between the static reliability oscillator and the compare circuit, the third counter to generate a static count; and

the compare circuit to compare the reference count with the dynamic count and the reference count with the static count.

6. The integrated circuit of claim 5, wherein the on-chip frequency compensation circuit further includes

a first prescaler coupled between the selectively enabled reliability oscillator and the first counter, the first prescaler to divide by N the number of oscillations in an oscillating signal from the selectively enabled reliability oscillator;

a second prescaler coupled between the dynamic reliability oscillator and the second counter, the second prescaler to divide by N the number of oscillations in an oscillating signal from the dynamic reliability oscillator; and

a third prescaler coupled between the static reliability oscillator and the third counter, the third prescaler to divide by N the number of oscillations in an oscillating signal from the static reliability oscillator.

7. The integrated circuit of claim 1, wherein the integrated circuit is a microprocessor.

8. An integrated circuit comprising:
one or more functional blocks; and
an on-chip frequency compensation circuit including

a selectively enabled reliability oscillator to generate a reference oscillating signal,

a static reliability oscillator to generate a DC bias degraded oscillating signal, and

a compare circuit coupled to the reliability oscillators, the compare circuit to compare the oscillating signals and to generate a frequency compensation signal in response to the comparison being greater than a predetermined threshold.

9. The integrated circuit of claim 8, wherein the on-chip frequency compensation circuit further includes

a first counter coupled between the selectively enabled reliability oscillator and the compare circuit, the first counter to generate a reference count;

a second counter coupled between the static reliability oscillator and the compare circuit, the second counter to generate a static count; and

the compare circuit to compare the reference count with the static count.

10. The integrated circuit of claim 9, wherein the on-chip frequency compensation circuit further includes

a first prescaler coupled between the selectively enabled reliability oscillator and the first counter, the first prescaler to divide by N the number of oscillations in an oscillating signal from the selectively enabled reliability oscillator; and

a second prescaler coupled between the dynamic reliability oscillator and the second counter, the second prescaler to divide by N the number of

oscillations in an oscillating signal from the static reliability oscillator.

11. The integrated circuit of claim 8, wherein the integrated circuit is a microprocessor.

12. An integrated circuit comprising:

one or more functional blocks to perform one or more functions; and

an on-chip frequency compensation circuit including

a first reliability oscillator including a selectively powered on ring oscillator to avoid transistor degradation, the first reliability oscillator to generate a reference oscillating signal on a first oscillation output,

a second reliability oscillator including a constantly powered ring oscillator to experience transistor degradation, the second reliability oscillator to generate a degraded oscillating signal on a second oscillation output,

a first counter having an input to couple to the first oscillation output, the first counter to generate a reference count on a first count output, and

a second counter having an input to couple to the second oscillation output, the second counter

to generate a degraded count on a second count output.

13. The integrated circuit of claim 12, wherein the on-chip frequency compensation circuit further includes

a first prescaler coupled between the first reliability oscillator and the first counter, the first prescaler to divide by N the number of oscillations in the reference oscillating signal; and

a second prescaler coupled between the second reliability oscillator and the second counter, the second prescaler to divide by N the number of oscillations in the degraded oscillating signal.

14. The integrated circuit of claim 12, wherein

the second reliability oscillator includes a constantly powered static ring oscillator to experience DC static transistor degradation, the degraded oscillating signal is an DC bias degraded oscillating signal on the second oscillation output, and the degraded count is a static count.

15. The integrated circuit of claim 12, wherein

the second reliability oscillator includes a constantly powered clocked ring oscillator to

experience AC dynamic transistor degradation, the degraded oscillating signal is an AC degraded oscillating signal on the second oscillation output, and the degraded count is a dynamic count.

16. The integrated circuit of claim 15, wherein the on-chip frequency compensation circuit further includes

a third reliability oscillator including a constantly powered static ring oscillator to experience DC static transistor degradation, the third reliability oscillator to generate a DC bias degraded oscillating signal on a third oscillation output, and

a third counter having an input to couple to the third oscillation output, the third counter to generate a static count on a third count output.

17. The integrated circuit of claim 16, wherein the on-chip frequency compensation circuit further includes

a first prescaler coupled between the first reliability oscillator and the first counter, the first prescaler to divide by N the number of oscillations in the reference oscillating signal,

a second prescaler coupled between the second reliability oscillator and the second counter, the

second prescaler to divide by N the number of oscillations in the dynamic oscillating signal, and

a third prescaler coupled between the third reliability oscillator and the third counter, the third prescaler to divide by N the number of oscillations in the static oscillating signal.

18. The integrated circuit of claim 13, wherein

the on-chip frequency compensation circuit further includes

a state machine to start and stop the counting by the counters.

19. The integrated circuit of claim 13, wherein

the first counter includes a count overflow output and a count enable input, the count overflow output being a stop signal is coupled to the count enable input to stop the first counter from counting further, and

the on-chip frequency compensation circuit further includes

a first synchronizer having an input coupled to the count overflow output and an output coupled to a count enable input of the second counter, the first synchronizer to synchronize the stop signal to stop the second counter from counting further.

20. The integrated circuit of claim 16, wherein

the first counter includes a count overflow output and a count enable input, the count overflow output being a stop signal is coupled to the count enable input to stop the first counter from counting further, and

the on-chip frequency compensation circuit further includes

a first synchronizer having an input coupled to the count overflow output and an output coupled to a count enable input of the second counter, the first synchronizer to synchronize the stop signal to stop the second counter from counting further, and

a second synchronizer having an input coupled to the count overflow output and an output coupled to a count enable input of the third counter, the second synchronizer to synchronize the stop signal to stop the third counter from counting further.

21. The integrated circuit of claim 12, wherein

a clock signal is coupled into a clock input of the second reliability oscillator.

22. The integrated circuit of claim 12, wherein

the integrated circuit is a microprocessor.

23. A method in an integrated circuit with functional blocks, the method comprising:

enabling measurement of ring oscillator frequencies of a trio of ring oscillators;

measuring a first frequency of a first ring oscillator having non-stressed transistors;

measuring a second frequency of a second ring oscillator having stressed transistors;

comparing the first frequency with the second frequency to determine a first measure of transistor degradation.

24. The method of claim 23, wherein

the stressed transistors of the second ring oscillator are dynamically stressed transistors.

25. The method of claim 23, wherein

the stressed transistors of the second ring oscillator are statically stressed transistors.

26. The method of claim 25, further comprising

measuring a third frequency of a third ring oscillator having dynamically stressed transistors; and

comparing the first frequency with the third frequency to determine a second measure of transistor degradation.

27. The method of claim 23 further comprising:

performing one or more functions with the functional blocks.

28. The method of claim 27, wherein

the functional blocks include an execution unit to execute instructions; and

the integrated circuit is a microprocessor.

29. The method of claim 23, wherein

the first ring oscillator and the second ring oscillator have substantially similar circuits.

30. The method of claim 29, wherein

the the second ring oscillator has degraded transistors; and

the first ring oscillator has transistors without degradation.

31. The method of claim 23, wherein

the comparing determines a new clock ratio,

and if the new clock ratio is less than an initial clock ratio multiplied by a guard band, then the new clock ratio is output to a clock generator.

32. The method of claim 31, further comprising

generating a clock signal using the new clock ratio.

33. A microprocessor integrated circuit comprising:

an execution unit to execute instructions; and

an integrated on-chip frequency compensation circuit including

a reference reliability oscillator to selectively generate a reference oscillating signal,

a degrading reliability oscillator to selectively generate a degraded oscillating signal, and

a measurement and comparison circuit coupled to the reliability oscillators, the measurement and comparison circuit to receive the reference oscillating signal and the degrading oscillating signal to generate a first measure of transistor degradation, the measurement and comparison circuit to receive the reference oscillating signal and the DC degraded oscillating signal to generate a second measure of transistor degradation.

34. The microprocessor integrated circuit of claim 33, wherein

the degrading reliability oscillator is a dynamic reliability oscillator that selectively generates an AC degraded oscillating signal.

35. The microprocessor integrated circuit of claim 33, wherein

the degrading reliability oscillator is a static reliability oscillator that selectively generates a DC degraded oscillating signal.

36. The microprocessor integrated circuit of claim 35, further comprising

a dynamic reliability oscillator to selectively generate an AC degraded oscillating signal, and

the measurement and comparison circuit to receive the reference oscillating signal and the AC degraded oscillating signal to generate a first measure of transistor degradation, the measurement and comparison circuit to receive the reference oscillating signal and the DC degraded oscillating signal to generate a second measure of transistor degradation.

37. The microprocessor integrated circuit of claim 36, wherein

the measurement and compare circuit further to compare the first measure of transistor degradation with the second measure of transistor degradation to determine a worst transistor degradation.

38. The microprocessor integrated circuit of claim 37, wherein

the measurement and compare circuit to generate a frequency compensation signal in response to the worst transistor degradation being greater than a predetermined level.